OIPE JG141
FEB 09 2004
PATENT & TRADEMARK OFFICE

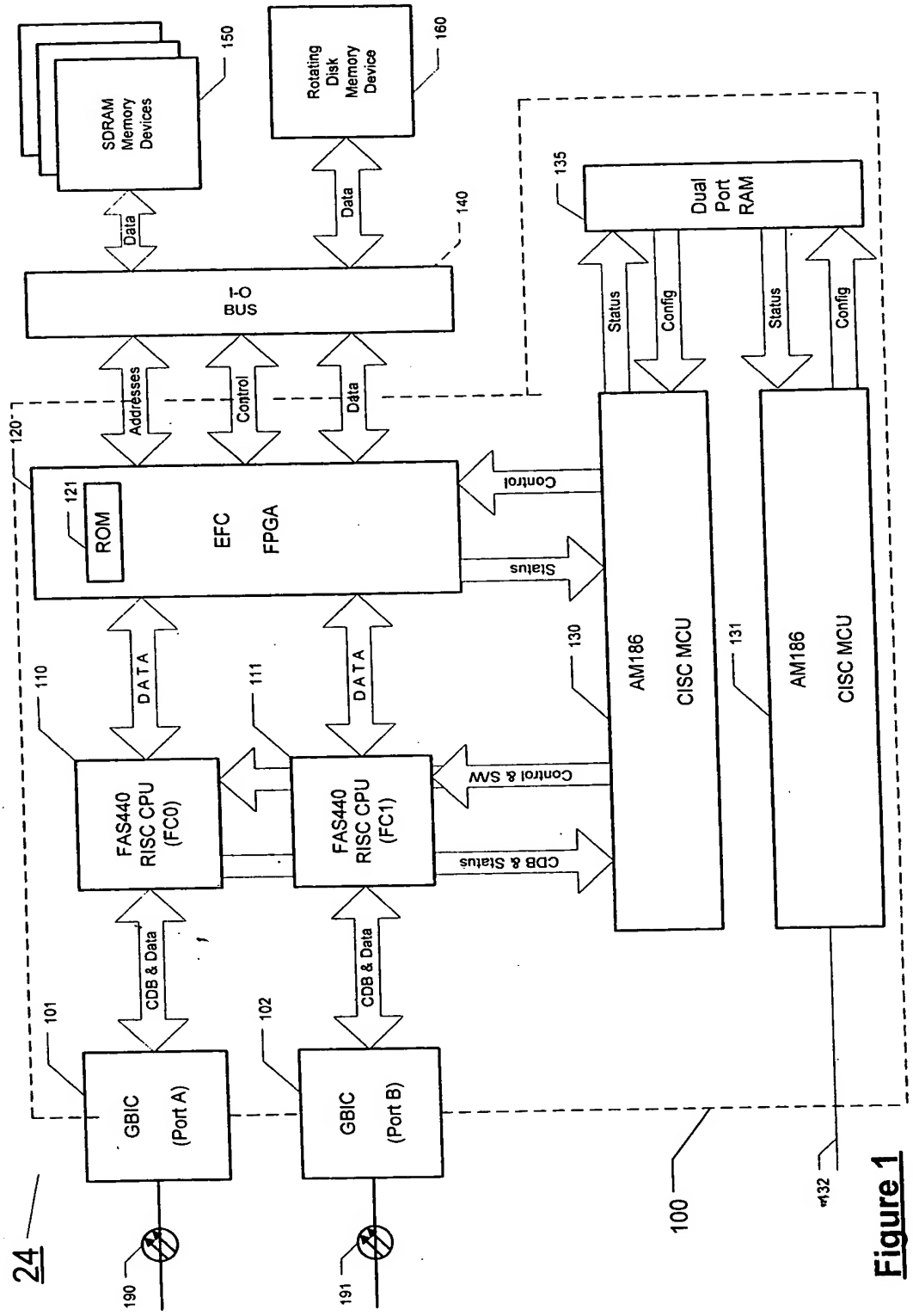


Figure 1

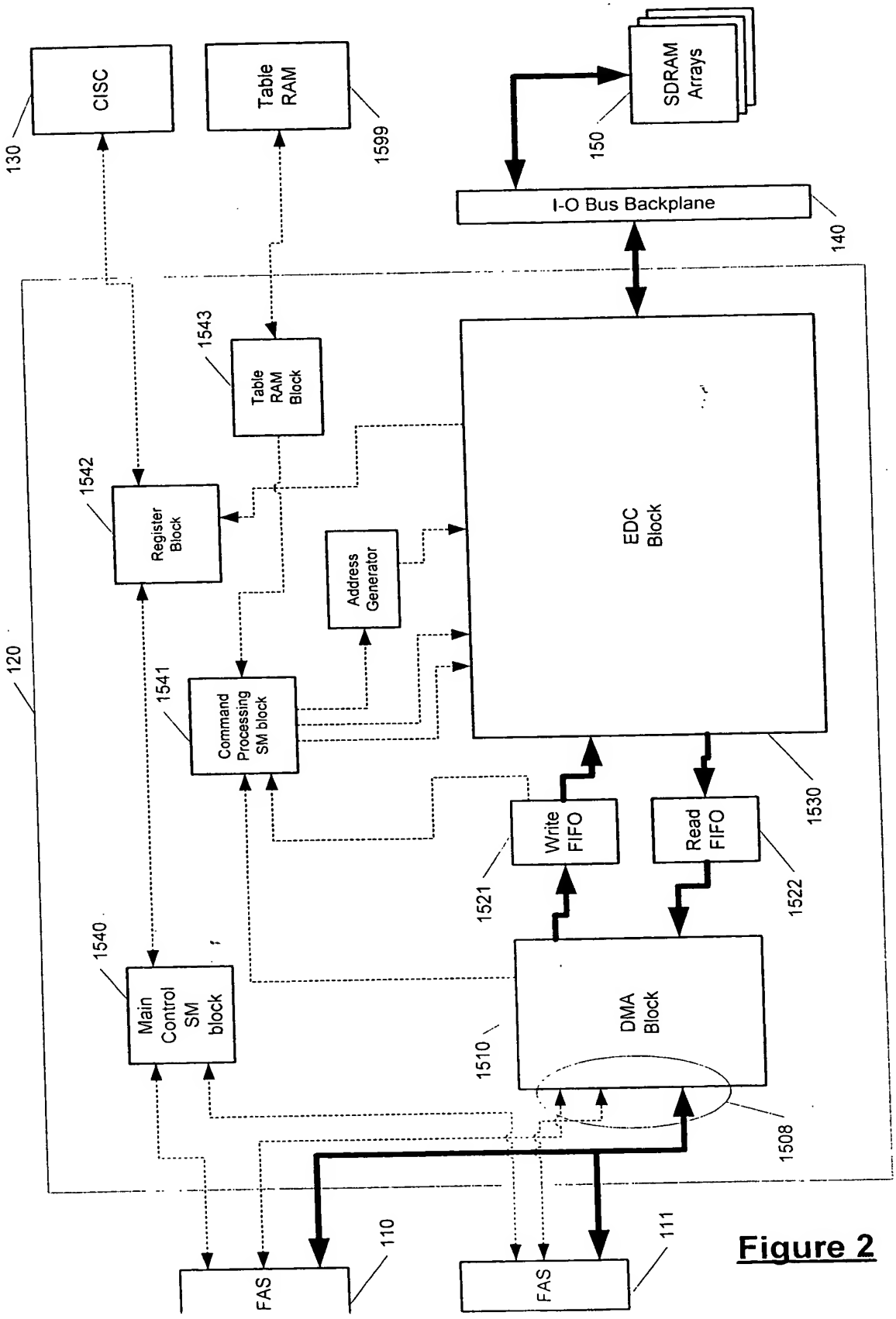
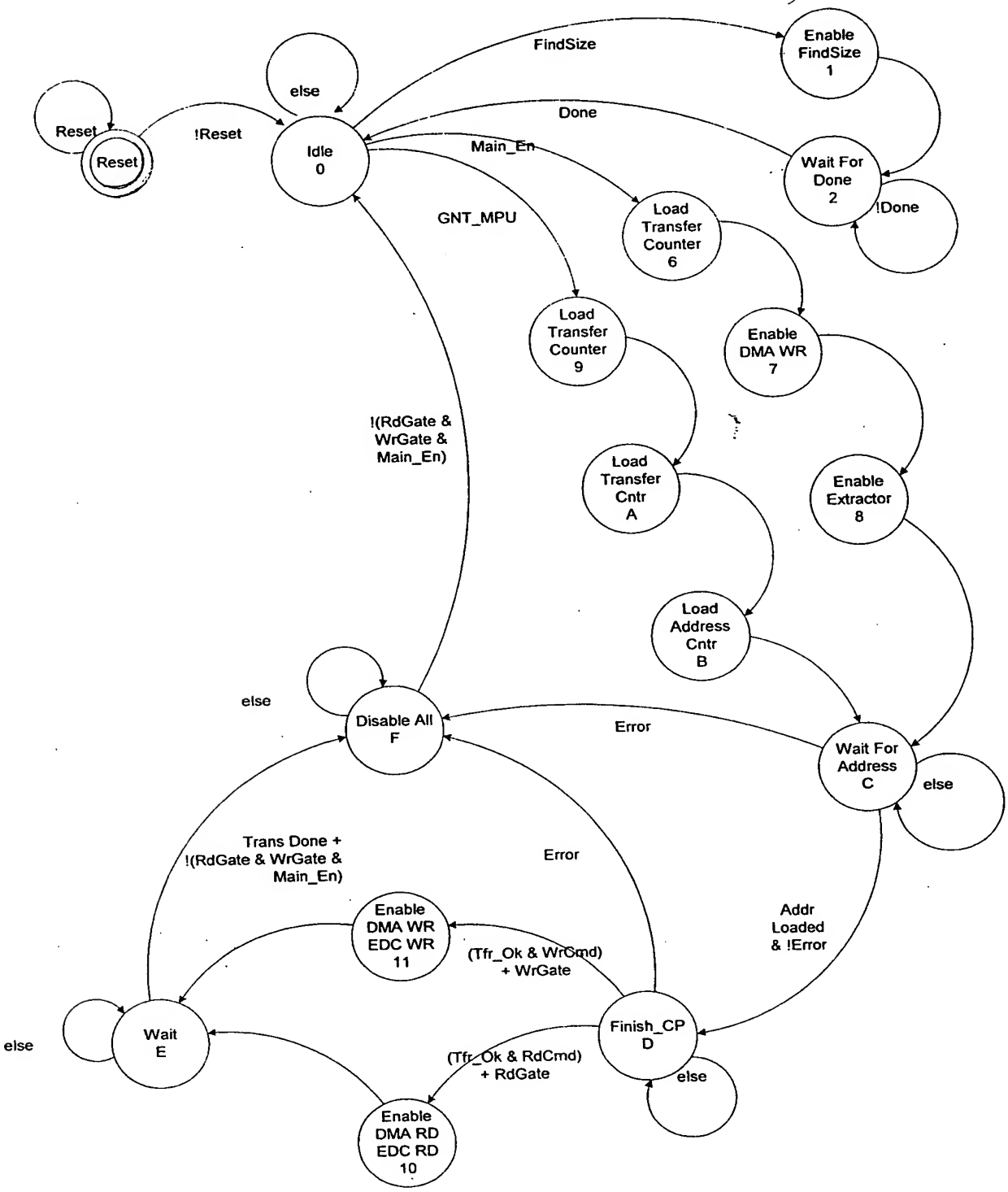
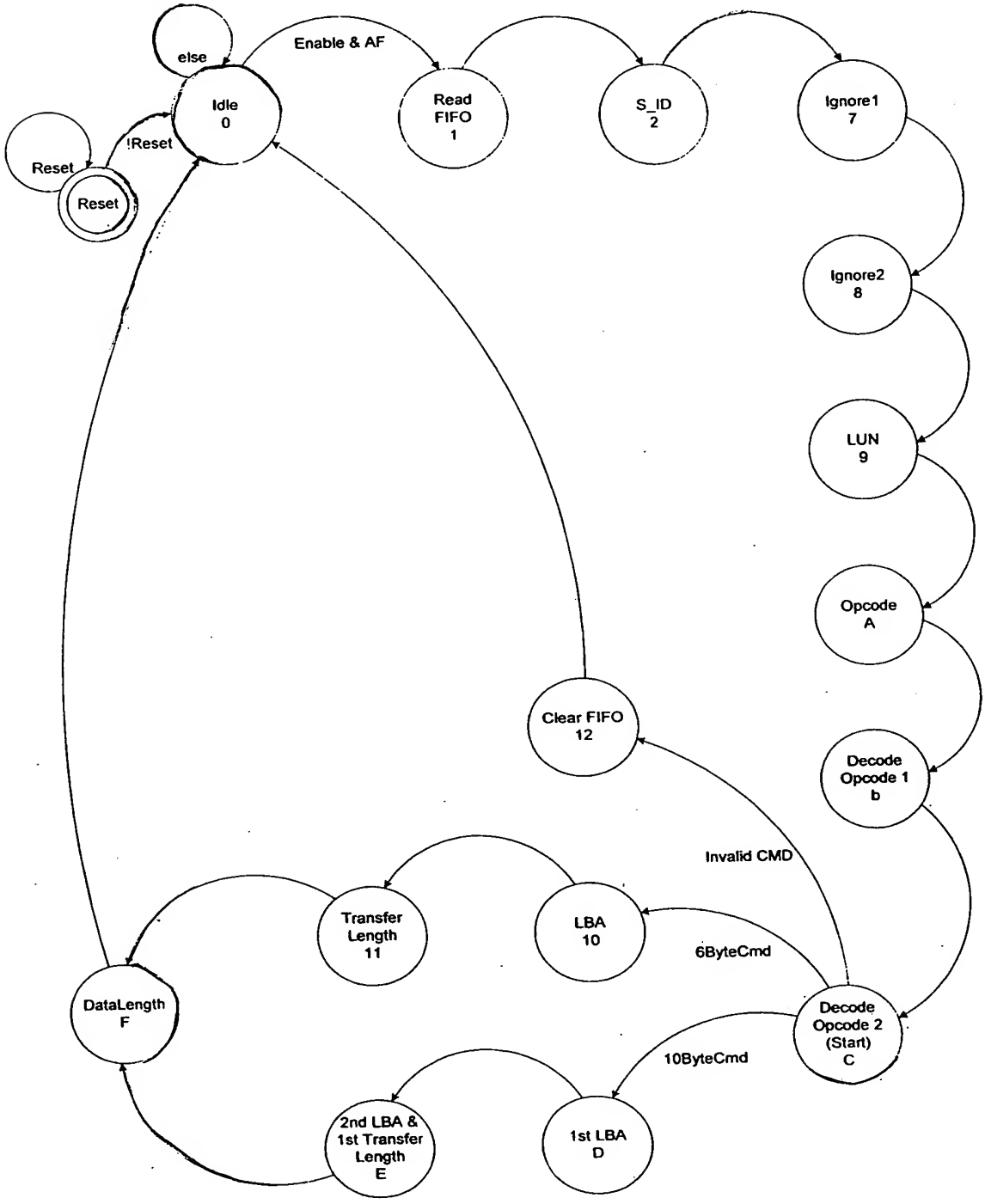

CISC
130
Table RAM
1599
SDRAM Arrays
150
I-O Bus Backplane
140
120
1543
Table RAM Block
1542
Register Block
Address Generator
EDC Block
1541
Command Processing SM block
1530
Write FIFO
Read FIFO
1521
1522
1540
Main Control SM block
DMA Block
1510
1508
FAS
110
FAS
111

Figure 2



Main State Diagram

Figure 3



Extractor State Diagram

Figure 4

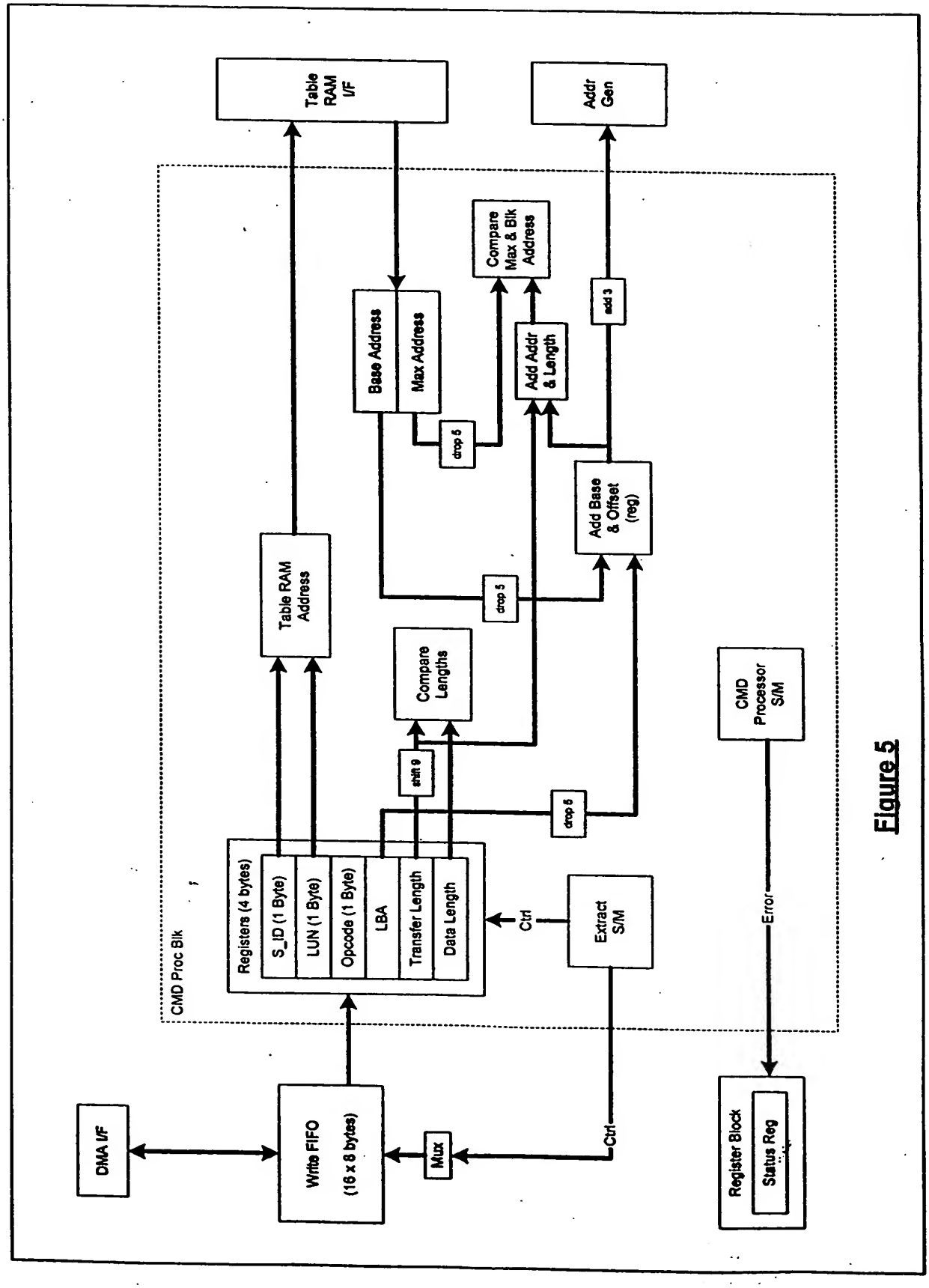


Table RAM I/F
Addr Gen
Compare Max & Blk Address
Base Address
Max Address
Add Addr & Length
add 3
drop 5
Add Base & Offset (reg)
Table RAM Address
drop 5
Compare Lengths
shift 9
drop 6
CMD Processor S/M
CMD Proc Blk
Registers (4 bytes)
S_ID (1 Byte)
LUN (1 Byte)
Opcode (1 Byte)
LBA
Transfer Length
Data Length
Ctrl
Extract S/M
Error
DMA I/F
Write FIFO (16 x 8 bytes)
Mux
Ctrl
Register Block
Status Reg

Figure 5

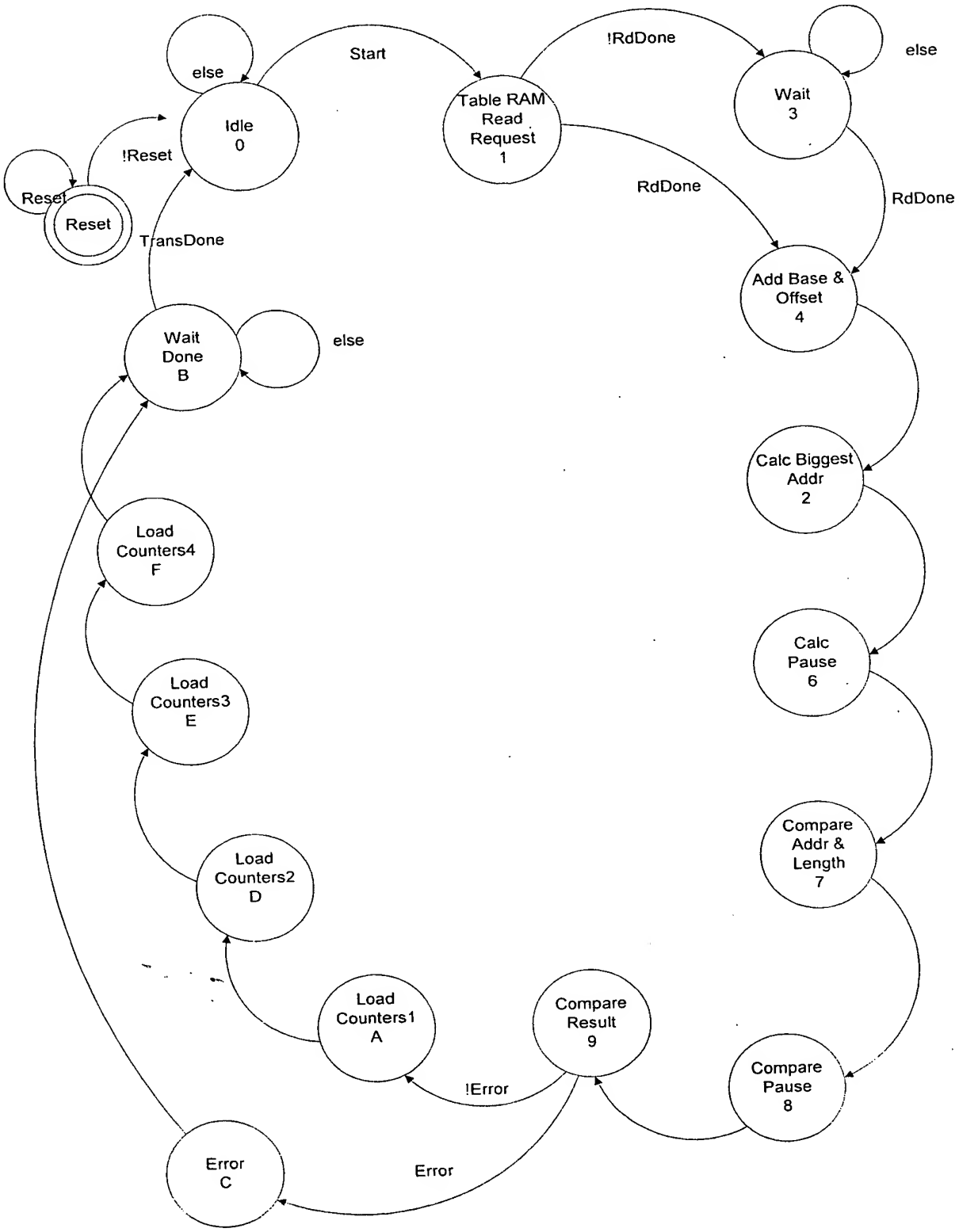


Figure 6

CMD Processor State Diagram

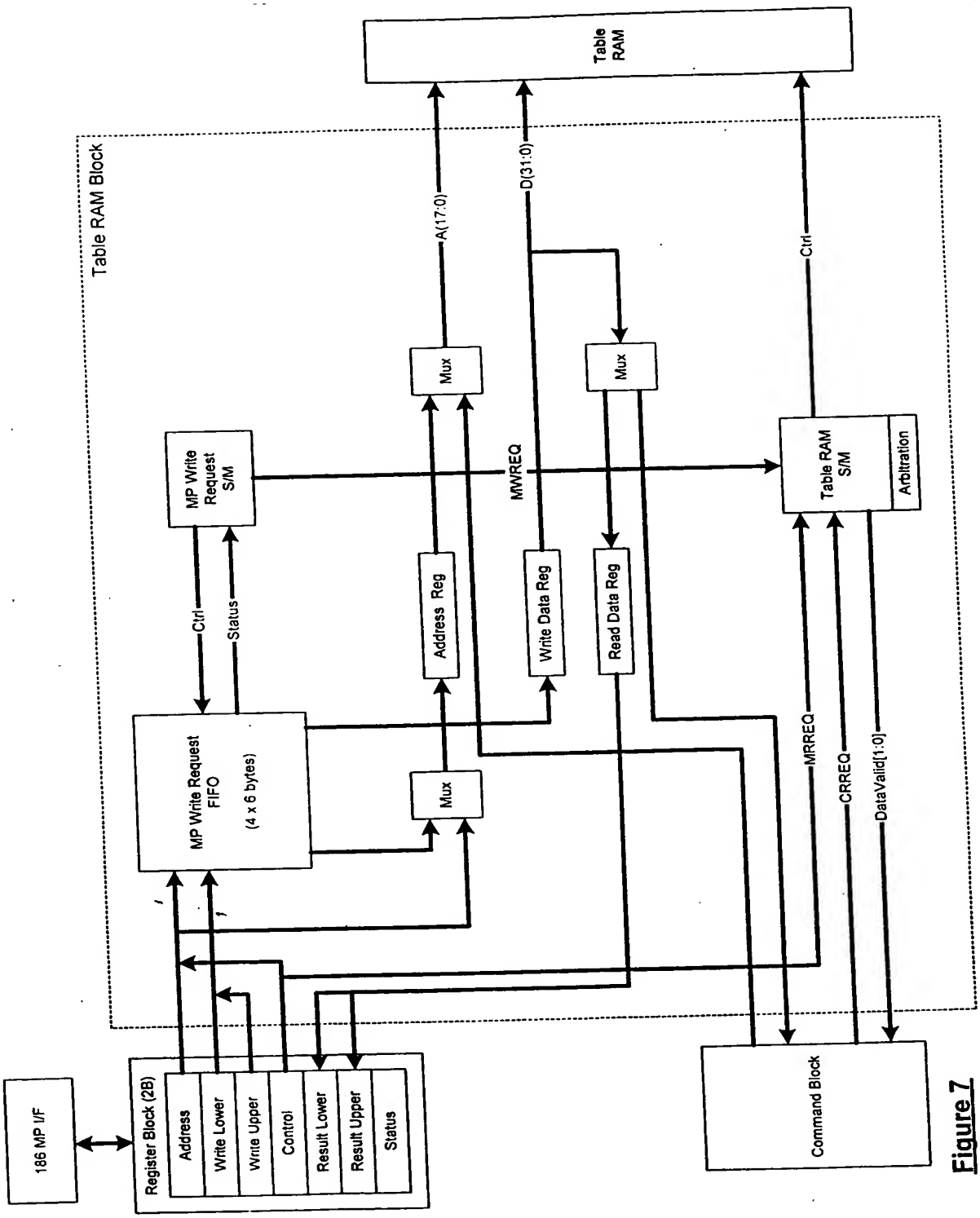
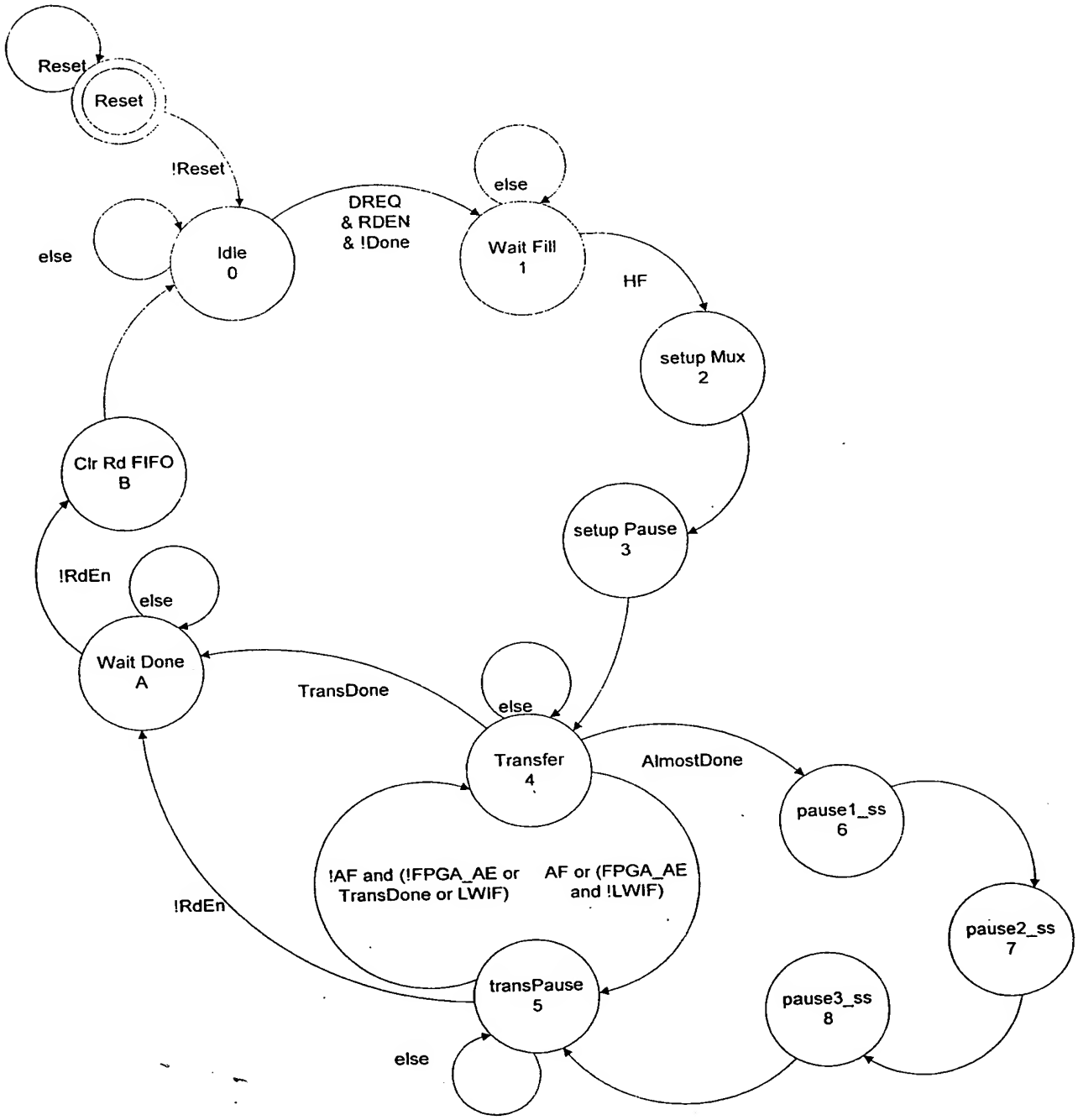


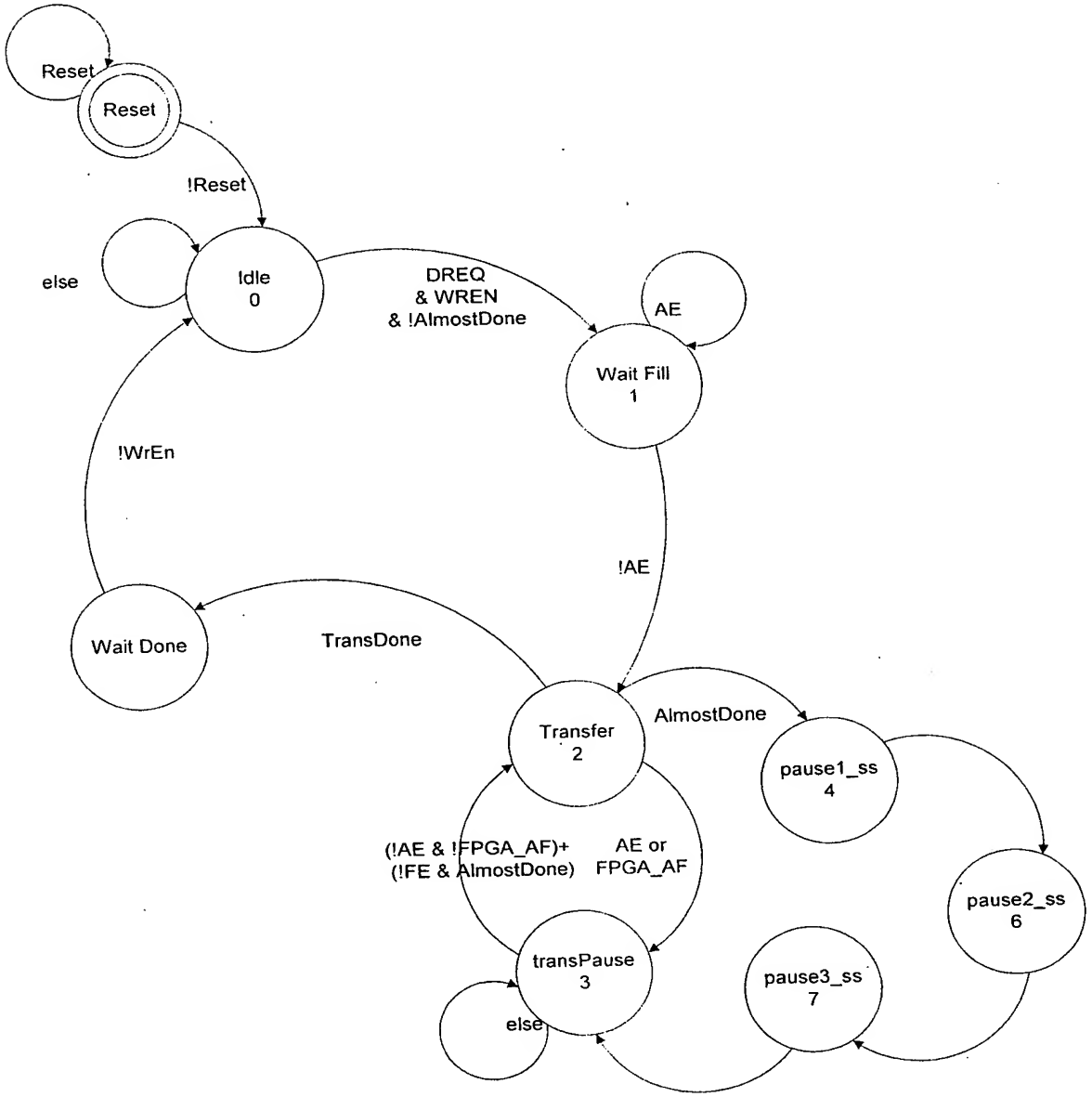
Table RAM
Table RAM Block
A(17:0)
D(31:0)
Ctrl
Mux
Mux
MP Write Request S/M
MWREQ
Table RAM S/M
Arbitration
Ctrl
Status
Address Reg
Write Data Reg
Read Data Reg
MP Write Request FIFO (4 x 6 bytes)
Mux
MRREQ
CRREQ
DataValid[1:0]
186 MP I/F
Register Block (2B)
Address
Write Lower
Write Upper
Control
Result Lower
Result Upper
Status
Command Block

Figure 7



DMA Read State Diagram

Figure 8



DMA Write State Diagram

Figure 9

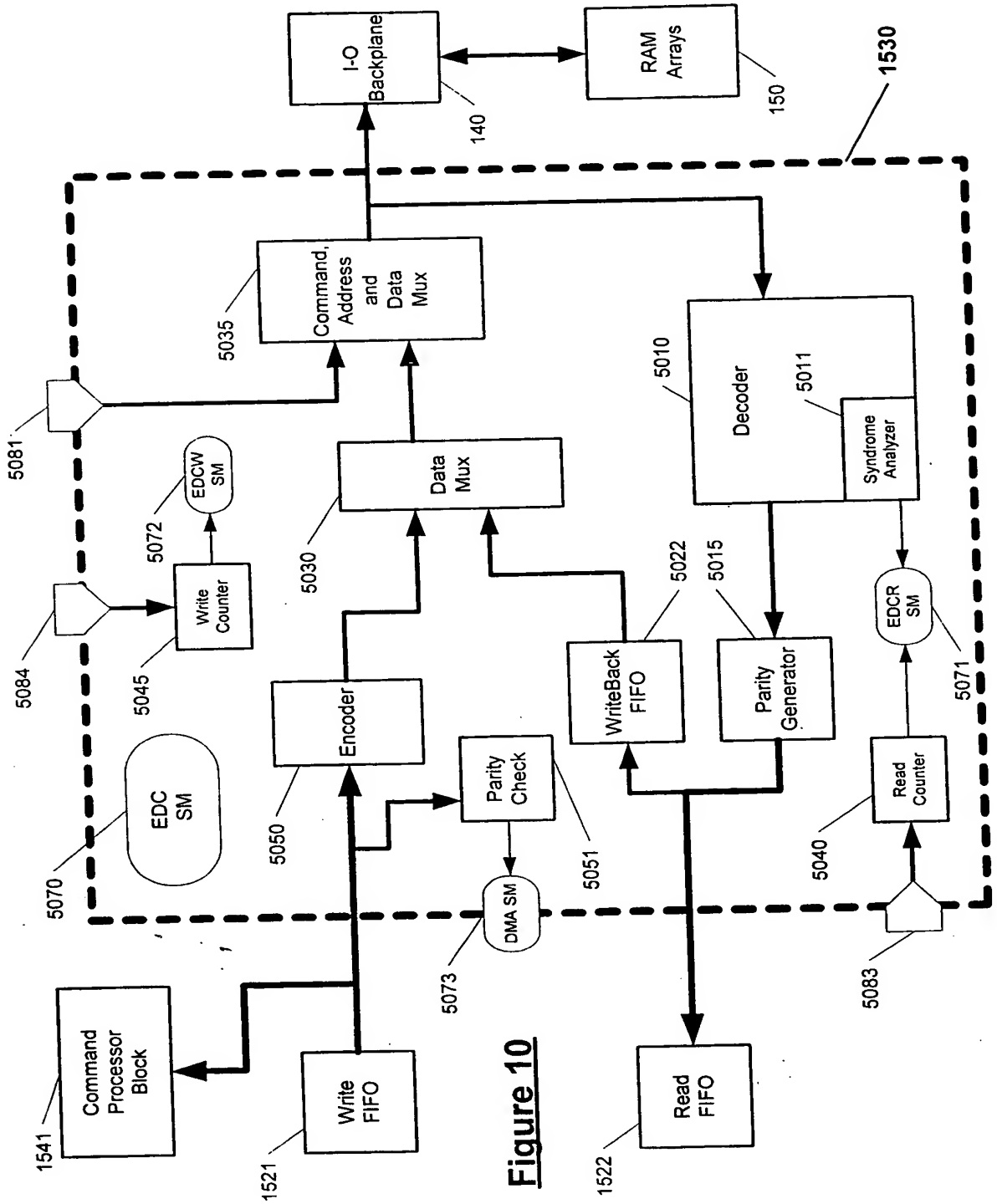
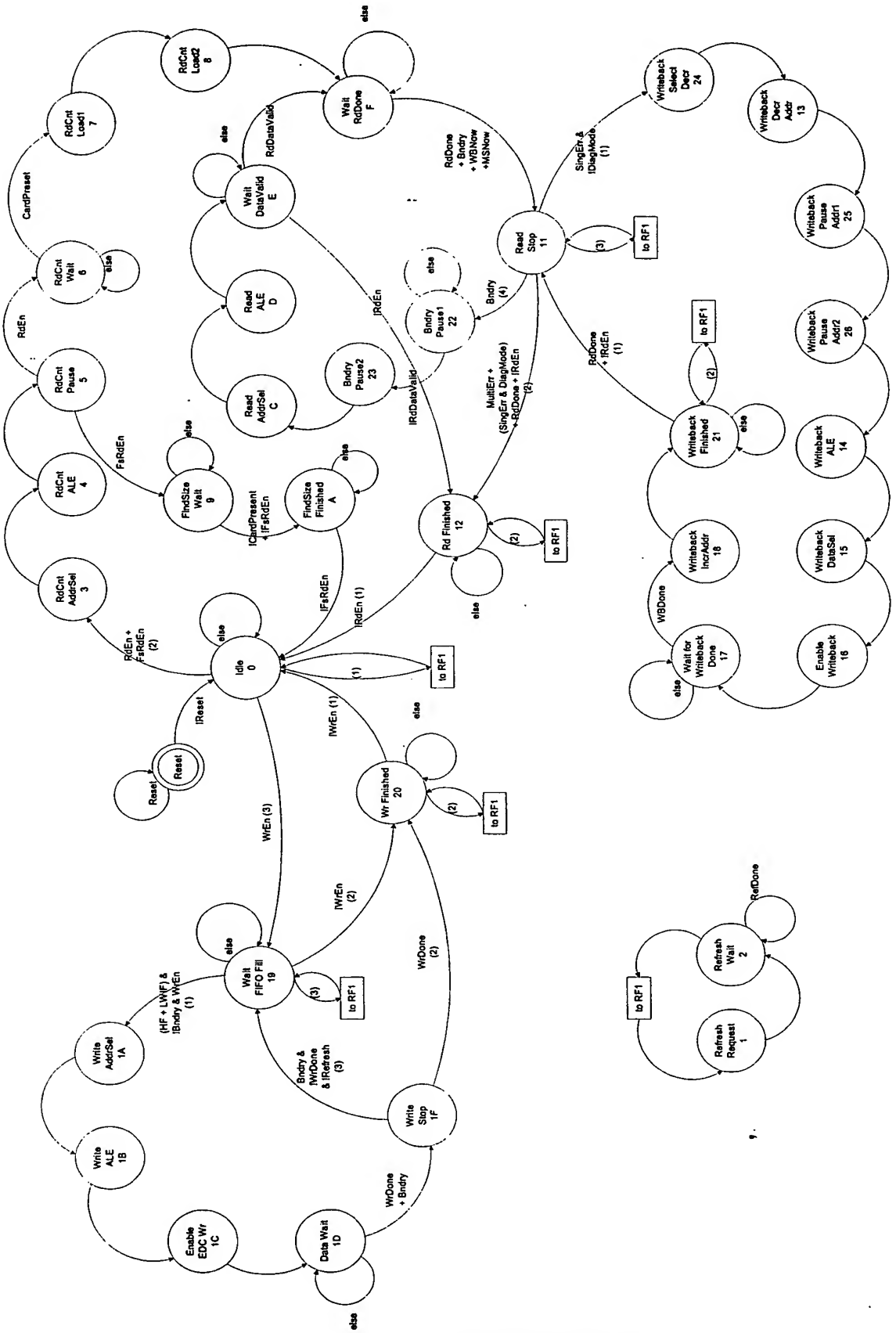
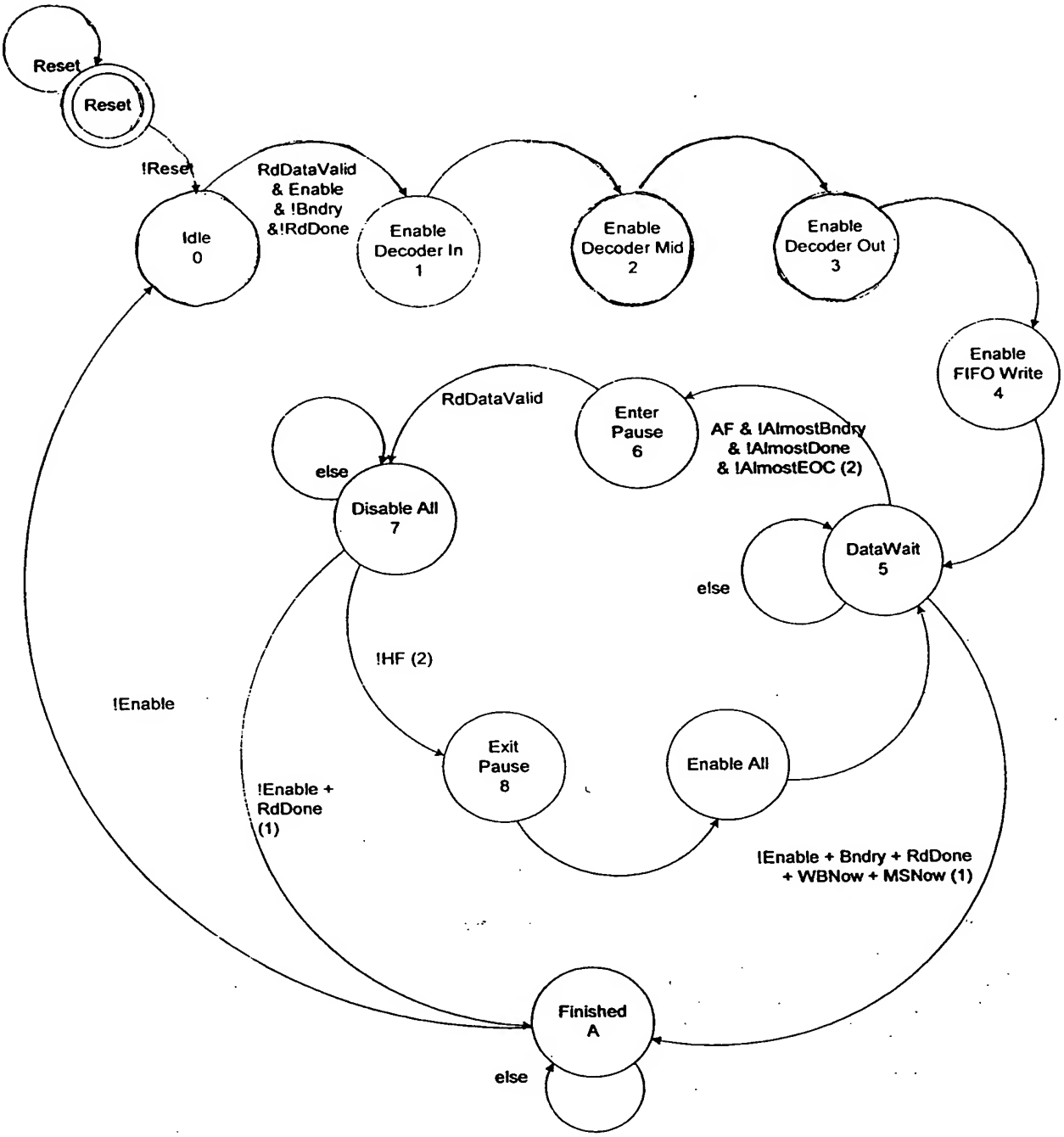

I-O Backplane
140
RAM Arrays
150
1530
Command, Address and Data Mux
5035
Decoder
5010
Syndrome Analyzer
5011
5081
EDCW SM
5072
Data Mux
5030
Write Counter
5045
5084
Encoder
5050
Parity Check
5051
WriteBack FIFO
5022
Parity Generator
5015
EDCR SM
5071
EDC SM
5070
DMA SM
5073
Read Counter
5040
5083
Command Processor Block
1541
Write FIFO
1521
Read FIFO
1522

Figure 10



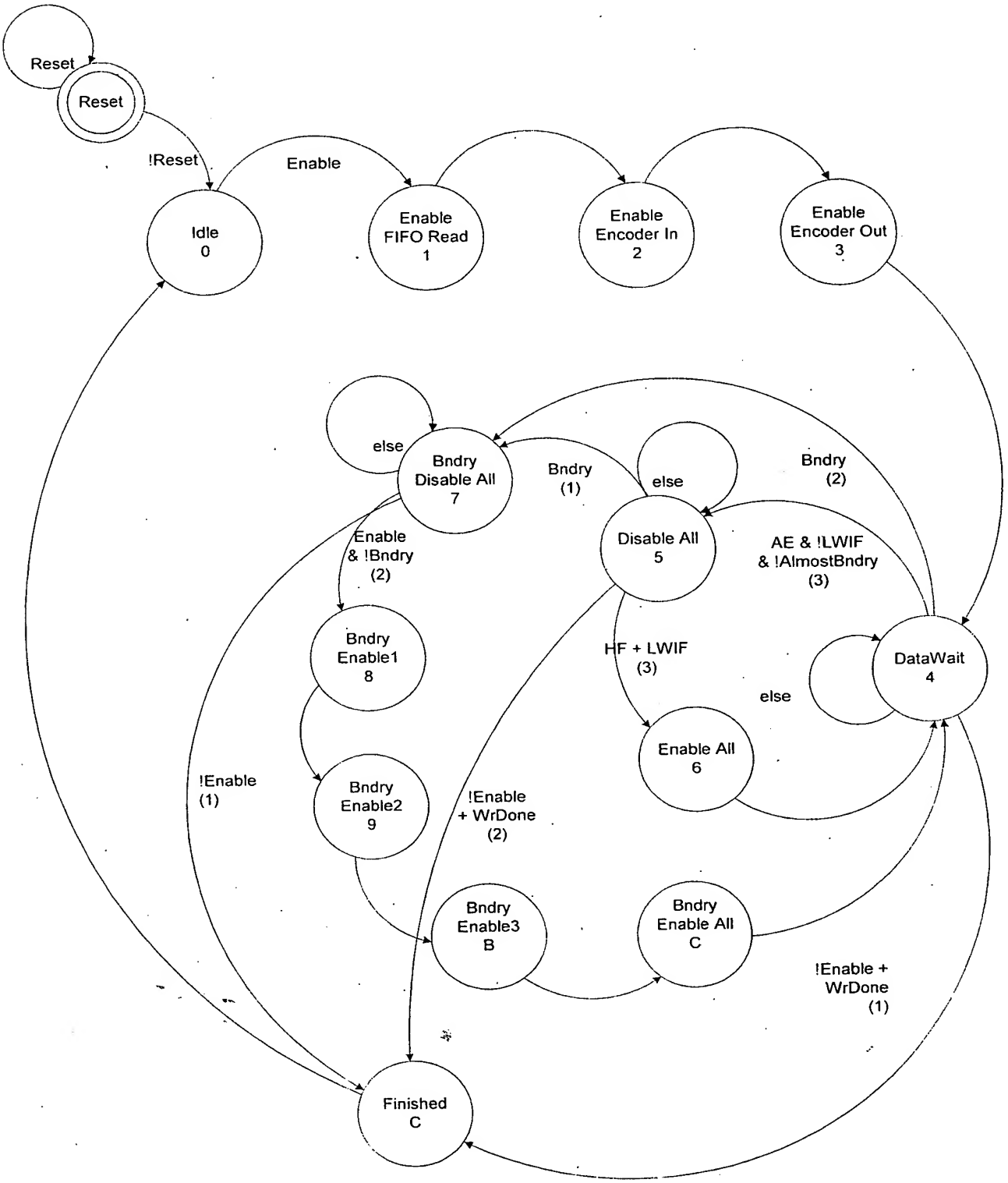
EDC State Diagram

FIGURE 11



EDC Read State Diagram

Figure 12



EDC Write State Diagram

Figure 13